REMARKS

The specification has been revised to correct various self-evident errors in spelling, typing, punctuation, reference-symbol usage, figure identification, and singular-versus-plural case. The missing verb "operates" has been inserted into the first sentence of paragraph 110. The missing reference symbol "164" has been inserted between "162" and "166" in the first sentence of paragraph 146 so that the corrected recitation "162, 164, 166" conforms to the later recitation "112, 114, 116" in that sentence.

The term "junction depletion 118" in paragraph 155 of the specification has been corrected to "junction depletion region 118" in conformity with usage of the term "junction depletion region 118" elsewhere in the specification. In paragraph 167, "threshold values V_X" has been corrected to "transition values V_X" since "value V_X" or "values V_X" is preceded by "transition" elsewhere in the specification, e.g., in the last sentence of paragraph 167.

The second sentence of paragraph 194 originally recited that "If electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to body region 100, electrode portion 112LA is doped more lightly n-type than is electrode portion 112LB". The third (next) sentence of paragraph 194 then recites that "In accordance with Eq. 33, gate portion 131B meets the requirement of having a higher value of zero-point gate-to-body threshold voltage V_{T0} than gate portion 131A".

Contrary to what was originally stated in the third sentence of paragraph 194, application of Eq. 33 (paragraph 165) to the situation in which electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to p-type body region 100 actually leads to the requirement that electrode portion 112LA be doped more heavily, rather than more lightly, than electrode portion 112LB in order for gate portion 131B to be of higher zero-point gate-to-body threshold voltage V_{T0} than gate portion 131A. Consequently, the second sentence of paragraph 194 has been corrected to recite that "If electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to body region 100, electrode portion 112LA is doped more heavily n-type than is electrode portion 112LB". This correction is supported by the third sentence of paragraph 195 (the next paragraph) that "If gate electrode layer 112L or 162L is divided into multiple portions of opposite conductivity type to body region 100 or 150 and of different N_{POLY} values, each gate

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electrode portion extends over part of plate region 100 or 152 or/and is continuous with another such gate electrode portion more heavily [emphasis added] doped than that gate electrode portion".

The fourth sentence of paragraph 194 recites that "The reverse dopant-concentration relationship arises if electrode portions 112LA and 112LB are both p-type and thus of the same conductivity type as body region 100". The fifth (next) sentence of paragraph 194 originally recited that "Per Eq. 33, electrode portion 112LA is doped more heavily p-type than is electrode portion 112LB".

Similar to what was stated above about the opposite conductivity-type situation in regard to the second and third sentences of paragraph 194 and contrary to what was originally stated in the fifth sentence of paragraph 194, application of Eq. 33 to the situation in which electrode portions 112LA and 112LB are both p-type and thus of the same conductivity type as p-type body region 100 leads to the requirement that electrode portion 112LA be doped more lightly, rather than more heavily, than electrode portion 112LB in order for gate portion 131B to be of higher zero-point gate-to-body threshold voltage V_{T0} than gate portion 131A. The fifth sentence of paragraph 194 has therefore been corrected to recite that "Per Eq. 33, electrode portion 112LA is doped more lightly p-type than is electrode portion 112LB". This further correction to paragraph 194 is supported by the fourth sentence of paragraph 195 (again the next paragraph) that "If electrode layer 112L or 162L is divided into multiple portions of the same conductivity type as body region 100 or 150 and of different N_{POLY} values, each gate electrode portion extends over part of plate region 102 or 152 or/and is continuous with another such gate electrode portion more lightly [emphasis added] doped than that gate electrode portion".

The terms "more lightly doped" and "more heavily doped" in paragraph 196 have been respectively corrected to "more heavily doped" and "more lightly doped" for the reasons given in the previous four paragraphs.

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For the case in which level shifter 234 is present, the last sentence of paragraph 268 originally specified that "The length of the V_{Rmin}-to-V_{Rmax} range is V_{HH} - V_{LL} - V_{LS}, the same as arises when shifter 234 is absent". However, paragraph 266 specifies that the length of the V_{Rmin}-to-V_{Rmax} range is V_{HH} - V_{LL} - V_{GBi} when shifter 234 is absent. Consequently, the last

sentence of paragraph 268 has been corrected to recite "The length of the V_{Rmin}-to-V_{Rmax} range is V_{HH} - V_{LL} - V_{Gbi}, the same as arises when shifter 234 is absent".

In paragraph 272, "plate electrode 162" has been changed to "gate electrode 162" since item 162 is the gate electrode. Finally, paragraph 317 has been revised to identify the U.S. patent number for the additional patent application cited in that paragraph.

Claims 1, 6, 9, 13, 15, 16, 20 - 22, 26, 27, 36, 42, 51 - 53, 55 - 57, and 59 have been amended. Non-elected Claims 61 - 68 have been cancelled. Dependent Claims 69 - 74 have been added to claim the invention with more particularity. Accordingly, Claims 1 - 60 and 69 - 74 are now pending.

Independent Claim 1 has been revised to make it clear that each inversion portion has a different zero-point threshold voltage than each other inversion portion by inserting the word "different" between "corresponding" and "zero-point threshold voltages of like sign". Word-omission and grammatical errors have been corrected in Claims 6, 9, 53, and 57. Claims 20 - 22, 26, 27, 42, and 51 - 53 have been amended to make it clear that the recited semiconductor material includes dopant by variously inserting "doped" before "semiconductor material", "non-monocrystalline semiconductor material", and "polycrystalline semiconductor material".

Independent Claim 53 has also been revised to provide that each gate electrode portion is continuous with at least one other gate electrode portion. This revision is supported by specification paragraphs 186 - 196 and by application Fig. 14 which illustrates gate electrode portions 112LA and 112LB as being continuous with each other.

Claim 53 has been further revised to provide that the gate electrode portions are "electrically shorted" to one another. For the case in which gate electrode portions 112LA and 112LB are of opposite conductivity type as particularly shown in the example of Fig. 14, the electrical shorting limitation is implemented with metallic layer 112U that contacts both of portions 112LA and 112LB. When portions 112LA and 112LB are of the same conductivity type, the electrical shorting limitation arises because portions 112LA and 112LB are continuous with each other regardless of whether metallic layer 112U is present or not.

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Claims 26, 27, 55, and 56 have been revised to conform to the changes made to specification paragraphs 194 and 196. Similar to how the location for the first gate dielectric portion is recited in Claim 35, Claim 36 has been revised to provide that the third gate dielectric portion extends to a location above the plate region. Claim 59 has been revised to delete the language relating to the "inversion portions" since no "inversion portions" are defined in Claim 59 or in independent Claim 53 from which Claim 59 directly depends.

Claims 1 - 5, 10 - 12, 29, 32, 33, 39, and 40 have been rejected under 35 USC 102(b) as anticipated by Sakai, U.S. Patent 4,529,994. This rejection is respectfully traversed.

Sakai discloses, in Fig. 3, a varactor often referred to here as Sakai's "MIS varactor". Sakai's MIS varactor is created from n-type semiconductor body 11 having an upper horizontal surface, two slanted surfaces 20 that respectively meet the opposite edges of the upper horizontal surface, two vertical side surfaces, and a lower horizontal surface. P-type regions 14 and 15 are provided in n-type semiconductor body 11 respectively along slanted surfaces 20. Control electrodes 16 and 17 respectively contact p-type regions 14 and 15 along slanted surfaces 20. Bottom electrode 18 contacts the n-type material of semiconductor body 11 along the bottom horizontal surface. Capacitance reading electrode 25 is situated on insulating layer 24 provided along the upper horizontal surface.

Item 19 in Fig. 3 of Sakai indicates a depletion layer that forms in the n-type material below insulating layer 24 along the p-n junctions between the n-type material and p-type regions 14 and 15. Although not shown in Fig. 3, depletion layer 19 presumably extends into p-type regions 14 and 15. The capacitive dielectric of Sakai's MIS varactor consists of depletion layer 19 and insulating layer 24. The capacitor plates consist of bottom electrode 18 and capacitance reading electrode 25.

Sakai applies a voltage between bottom electrode 18, on one hand, and control electrodes 16 and 17, on the other hand, sufficient to reverse bias the p-n junctions formed between the n-type material and p-type regions 14 and 15. The thickness of depletion layer 19 varies as a function of the reverse bias voltage. This causes the capacitance, as measured between capacitance reading electrode 25 and bottom electrode 18, to vary in a corresponding manner.

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Independent Claim 1 is directed to a structure containing a varactor in which an inversion layer occurs in a body region along a gate dielectric layer below a gate electrode. Claim 1 recites, in material part, that the inversion layer comprises "multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign", that each inversion portion largely appears/disappears "when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero", and that each inversion portion meets "the varactor's plate region or/and" is "continuous with another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion".

The Examiner alleges that Sakai discloses "an inversion layer 19 occurring in the body region along the gate dielectric layer below the gate electrode, the inversion layer comprising multiple variably appearing inversion portions (at the middle and the sides of region 19, where there are different thickness)". This is incorrect. Item 19 in Sakai is a depletion layer, not an inversion layer.

Depletion and inversion layers are two very different, basically opposite, semiconductor phenomena. A depletion layer is essentially an electrical insulator. This insulating characteristic enables a depletion layer to be used as capacitive dielectric in a capacitor or varactor. In contrast, an inversion layer is essentially an electrical conductor and is therefore unsuitable for use as capacitive dielectric.

To further understand the differences between inversion and depletion layers, it is helpful to briefly review certain basic semiconductor device physics. A piece of doped semiconductor material consists of neutral atoms of the semiconductor material, singly charged atoms of semiconductor dopant, and mobile charge carriers. The singly charged atoms of dopant are commonly referred to as bound charges because they are immobile. The bound charges are positively charged for n-type dopant formed with electron donor atoms. For p-type dopant formed with electron acceptor atoms, the bound charges are negatively charged.

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The mobile charge carriers consist of negatively charged electrons and positively charged holes (basically the absence of electrons). The mobile charge carriers are further

classified as majority charge carriers and minority charge carriers. For n-type semiconductor material, the majority charge carriers are electrons. The minority charge carriers in n-type semiconductor material are holes. The reverse applies to p-type semiconductor material for which the majority carriers are holes while the minority carriers are electrons.

A piece of doped semiconductor material not subjected to any external electrical potential difference (voltage) is electrically neutral. The concentration (or density) of majority charge carriers in doped electrically neutral semiconductor material is much higher, typically many orders of magnitude higher, than the concentration of minority charge carriers in the electrically neutral semiconductor material.

A depletion layer, sometimes referred to as a space-charge layer, is a doped semiconductor region substantially devoid of mobile majority charge carriers. For instance, when a depletion layer is formed in n-type semiconductor material for which the n-type dopant atoms are electron donors, the depletion layer is substantially devoid of electrons, the majority charge carriers for electrically neutral n-type semiconductor material. A depletion layer formed in p-type semiconductor material whose p-type dopant atoms are electron acceptors is substantially devoid of holes, the mobile majority charge carriers for electrically neutral p-type semiconductor material.

The bound charges formed by the singly charged dopant atoms in a depletion layer cause the layer to be positively charged, in the case of n-type semiconductor material, or negatively charged, in the case of p-type semiconductor material. Because the bound charges are immobile, they cannot conduct electricity. In the absence of a suitable electrical potential difference that causes charge to be injected into a depletion layer, the substantial absence of majority charge carriers in a depletion layer causes it to have a very weak capability for conducting electricity. Hence, a depletion layer is effectively an electrical insulator.

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An inversion layer is a thin doped semiconductor region in which the concentration of minority charge carriers is considerably greater than what would occur in otherwise identical electrically neutral semiconductor material. Taking note of the fact that mobile charge carriers, both majority carriers and minority carriers, are continually being thermally created in semiconductor material, an inversion layer forms in a thin portion of a depletion layer, e.g., along the interface between the depletion layer and a region of electrically insulating

material, when an electrical potential difference is applied across the semiconductor material in such a way as to attract minority charge carriers to the semiconductor region that constitutes the inversion layer.

For n-type semiconductor material whose majority charge carriers are electrons, the mobile charge carriers in an inversion layer formed in the n-type semiconductor material are <u>mainly</u> holes. The opposite occurs in p-type semiconductor material whose majority charge carriers are holes. That is, the mobile charge carriers in an inversion layer formed in the p-type semiconductor material are <u>mainly</u> electrons. Because the mobile charge carriers in an inversion layer formed in a piece of doped semiconductor material consist <u>mainly</u> of <u>minority</u> carriers for that doped semiconductor material, the conductivity type of the doped semiconductor region which forms the inversion layer is effectively <u>inverted</u> from the conductivity type of the electrically neutral portion(s) of the doped semiconductor material.

An inversion layer formed in a piece of doped semiconductor material is commonly considered to be in weak inversion when the concentration of minority charge carriers in the inversion layer is less than the net concentration of dopant atoms in the inversion layer. Strong inversion arises when the concentration of minority carriers in the inversion layer is greater than the net concentration of dopant atoms in the inversion layer. In either case, the presence of a substantial concentration of minority carriers enables the inversion layer to conduct electricity quite well. Accordingly, an inversion layer is effectively an electrical conductor.

Nowhere does Sakai mention inversion or in any way indicate that an inversion layer is formed at any location in Sakai's MIS varactor. Applicant's Attorney notes, nonetheless, that an inversion layer could be formed in depletion layer 19 along the bottom of insulating layer 24 if appropriate voltages were applied to electrodes 16 - 18 and 25. Since (the illustrated portion of) depletion layer 19 is doped n-type, the charge carriers in such an inversion layer would mainly be holes, the minority carriers for n-type semiconductor material. The inversion layer would laterally terminate at p-type regions 14 and 15.

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Even if Sakai's MIS varactor were operated under conditions that cause such an inversion layer to form, the inversion layer would appear at substantially <u>single</u> instances of time and would disappear at substantially <u>single</u> instances of time. Contrary to what is

required by Claim 1, such an inversion layer in the MIS varactor would not comprise multiple variably appearing inversion portions. Likewise, Sakai's MIS varactor would not meet the requirement of Claim 1 that the inversion portions be characterized by different zero-point threshold voltages of like sign or that each inversion portion largely appear/disappear when the gate-to-body voltage passed through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero.

Nor would Sakai's MIS varactor satisfy the requirement of Claim 1 that each inversion portion meet the plate region or/and be continuous with another inversion portion of lower zero-point threshold voltage than that inversion portion. Consequently, Sakai does not anticipate Claim 1.

Furthermore, the Examiner has analogized control electrode 16, bottom electrode 18, and capacitance reading electrode 25 of Sakai respectively to the plate, body, and gate electrodes of Claim 1. As mentioned above, Sakai measures the capacitance of the MIS varactor between capacitance reading electrode 25 and bottom electrode 18. That is, Sakai measures the capacitance between the electrodes analogized by the Examiner to the gate and body electrodes of Claim 1.

Sakai does not disclose any circuitry that actually utilizes any of Sakai's varactors. However, Sakai clearly intends to employ each of its varactors, including the MIS varactor, in some electronic circuitry. Since Sakai measures the capacitance of the MIS varactor between "gate" electrode 25 and "body" electrode 18, the circuitry that employs the MIS varactor would have a capacitance signal path in which gate electrode 25 and body electrode 18 are situated.

In addition to the varactors characteristics, Claim 1 recites that the claimed structure includes "further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor" and that "the plate and body electrodes" are "situated in the capacitance signal path". In particular, Claim 1 requires that the plate electrode be one of the electrodes situated in the capacitance signal path of the further electronic circuitry. Since "gate" electrode 25 and "body" electrode 18 would be situated in capacitance signal path of the circuitry that employs Sakai's MIS varactor, control electrode 16 (or 17) analogized by the Examiner to the

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plate electrode of Claim 1, would not be in the capacitance signal path of that circuitry. Sakai therefore fails to explicitly or inherently meet the requirement of Claim 1 that the plate electrode be in the capacitance signal path. This is a further reason why Sakai does not anticipate Claim 1.

Nothing in Sakai would provide a person skilled in the art with any motivation or incentive for modifying Sakai's MIS varactor so that it produces an inversion layer consisting of multiple variably appearing inversion portions. Attempting to so modify Sakai's MIS varactor would not yield any improvement in varactor performance. In fact, the varactor would likely be degraded. Nor would there be any reason for reconfiguring Sakai's MIS varactor so that "plate" electrode 16 (or 17) and body electrode 18 are in the capacitance signal path of electronic circuitry that employs Sakai's MIS varactor. Claim 1 is thus patentable over Sakai.

Claims 2 - 5, 10 - 12, 29, 32, and 33 all depend (directly or indirectly) from Claim 1. Dependent Claims 2 - 5, 10 - 12, 29, 32, and 33 are thus patentable over Sakai for the same reasons as Claim 1.

Additionally, Sakai fails to disclose the further limitation of every one of dependent Claims 2 - 5, 10 - 12, 29, 32, and 33. The further subject matter recited in Claims 2 - 5, 10 - 12, 29, 32, and 33 makes them separately patentable over Sakai.

Moving to independent Claim 39, it is directed to a structure containing a varactor in which a surface depletion region of a body region extends along a gate dielectric layer below a gate electrode. Claim 39 specifies that the surface depletion region comprises "multiple surface depletion portions of different respective average net dopant concentrations" and that each of the surface depletion portions meets the plate region or/and is "continuous with a surface depletion portion more lightly doped than that surface depletion portion".

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A section of depletion layer 19 in Sakai's MIS varactor extends along insulating layer 24 below capacitance reading electrode 25. This section of layer 19 does constitute a surface depletion region. However, nowhere does Sakai disclose or in any way suggest that depletion layer 19, or the surface depletion section extending along insulating layer 24 below electrode 25, consists of multiple surface depletion portions of different average net dopant concentrations. Nor is it inherent that depletion layer 19, or the indicated surface depletion

section, consists of multiple surface depletion portions of different average net dopant concentrations.

The variation in the thickness of depletion layer 19 in Sakai's MIS varactor arises from geometrical factors and/or the voltages applied to electrodes 16 - 18 and 25, not from configuring layer 19, or the surface depletion section extending along insulating layer 24 below electrode 25, as multiple surface depletion portions of different average net dopant concentrations. Sakai fails to meet the limitation of Claim 39 that the surface depletion region comprise multiple surface depletion portions of different average net dopant concentrations. Consequently, Sakai does not anticipate Claim 39.

Similar to Claim 1, Claim 39 also recites that the claimed structure includes "further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor" and that "the plate and body electrodes" are "situated in the capacitance signal path". For the reasons presented above in connection with the further electronic circuitry of Claim 1, Sakai does not explicitly or inherently meet the requirement of Claim 39 that the plate electrode be situated in the capacitance signal path of electronic circuitry the utilizes the recited varactor. This is another reason why Sakai does not anticipate Claim 39.

Nothing in Sakai would provide a person skilled in the art with any suggestion or motivation for modifying Sakai's MIS varactor so that the depletion section extending along insulating layer 24 below electrode 25 contains multiple surface depletion portions of different average net dopant concentrations. Modifying Sakai's MIS varactor in such a manner might degrade the varactor performance and, in any case, would not enhance the varactor performance.

Furthermore, modifying Sakai's MIS varactor so that the surface depletion section extending along insulating layer 24 below electrode 25 consists of multiple surface depletion portions of different average net dopant concentrations would increase the fabrication complexity and attendant fabrication costs. Since the varactor performance would not be improved, there would be no economic justification for producing a varactor of greater complexity and higher cost. A person skilled in the art would have absolutely no reason for so modifying Sakai's varactor. Also, nothing in Sakai would provide a person skilled in the

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art with any motivation for reconfiguring Sakai's MIS varactor so that "plate" electrode 16 (or 17) and "body" electrode 18, rather than "gate" electrode 25 and "body" electrode 18, are in the capacitance signal path of electronic circuitry that utilizes Sakai's MIS varactor. Hence, Claim 39 is patentable over Sakai.

Claim 40 depends from Claim 39 and is thus patentable over Sakai for the same reasons as Claim 39. Also, Sakai does not disclose or suggest the further limitation of Claim 40. For this reason, Claim 40 is separately patentable over Sakai.

Claims 6, 7 - 9, and 34 - 37 have been rejected under 35 USC 103(a) as obvious based on Sakai in view of Hattori, U.S. Patent Publication 2002/0036311 A1. This rejection is respectfully traversed.

Hattori discloses a power semiconductor device in which pinchoff is shifted away from a p-type base location near n^+ emitter 6 to a p-type base location near n-type base 1 by making gate dielectric layer 3/10 thicker above the p-type base location near n-type base 1. According to Hattori, configuring gate dielectric layer 3/10 in this manner causes the collector-to-emitter voltage to be reduced so as to reduce the saturation current.

Claim 6, which depends from Claim 1, recites that "the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses" and that each gate dielectric portion is "situated above at least where a different corresponding one of the inversion portions occurs". Claim 7, which depends from Claim 6, recites that "each gate dielectric portion extends to a location above the plate region or/and is continuous with a gate dielectric portion thinner than that gate dielectric portion".

Independent Claim 34 is directed to a structure containing a varactor in which a gate dielectric layer lies between a gate electrode and a body region. Similar to Claims 6 and 7, Claim 34 recites that the gate dielectric layer comprises "multiple gate dielectric portions of different respective thicknesses" and that each gate dielectric portion extends "to a location above the plate region or/and" is "continuous with a gate dielectric portion thinner than that gate dielectric portion". Hattori does indeed disclose a gate dielectric layer consisting of multiple portions of different thicknesses. However, absolutely <u>nothing</u> in Sakai and/or Hattori would provide a person skilled in the art with any suggestion or reason for configuring insulating layer 24 in Sakai's MIS varactor as multiple portions of different

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thicknesses. Inasmuch as Sakai lacks an inversion layer consisting of multiple variably appearing portions of different zero-point threshold voltages, Sakai has no need for a gate dielectric layer formed with multiple portions of different thicknesses.

Modifying Sakai's insulating layer 24 so as to consist of multiple portions of different thicknesses would not cause Sakai's MIS varactor to perform better. In fact, so configuring Sakai's MIS varactor would likely cause the varactor performance to be degraded.

Furthermore, modifying Sakai's MIS varactor so that insulating layer 24 consists of multiple portions of different thicknesses would increase the manufacturing complexity and cost. Without a performance improvement, such an increase in manufacturing complexity and cost would not be economically justifiable. Accordingly, a person skilled in the art would absolutely not apply the teachings of Hattori to Sakai in an effort to reach the subject matter of any of Claims 6, 7, and 34. Claims 6, 7, and 34 are thus patentable over Sakai and Hattori.

Claim 9 depends from Claim 7. Claims 35 - 37 all depend (directly or indirectly) from Claim 34. Consequently, dependent Claims 9 and 35 - 37 are patentable over Sakai and Hattori for the same reasons as Claims 6, 7, and 34.

Neither Sakai nor Hattori discloses the further limitation of any of dependent Claims 9, 36, and 37. Separate bases are thereby provided for allowing Claims 9, 36, and 37 over Sakai and Hattori.

Claims 13, 17, 18, 42, 44, 45, 53, 57, and 58 have been rejected under 35 USC 103(a) as obvious based on Sakai in view of Tada, Japanese Patent Publication 4-199682. Claims 19 and 46 have been rejected under 35 USC 103(a) as obvious based on Sakai and Tada in view of Iwamuro, U.S. Patent 5,659,185. Claims 20, 21, 51, and 52 have been rejected under 35 USC 103(a) as obvious based on Sakai and Tada in view of Pramanick et al. ("Pramanick"), U.S. Patent 6,165,902. These rejections are respectfully traversed.

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Tada discloses a semiconductor device, apparently a transistor, in which top gate electrode 8 is electrically insulated from a bottom gate electrode consisting of p-type layer 4 and n-type layer 5 that meet each other to form a p-n junction. Bottom gate electrode 4/5 is

electrically insulated from semiconductor substrate 1, specifically from doped layer 2 of substrate 1.

Iwamuro discloses a thyristor in which a pair of gate electrodes 12 are electrically connected to each other. At col. 5, Iwamuro provides that gate electrodes 12 are deposited on gate oxide film 14. Although not explicitly stated in Iwamuro, electrodes 12 are presumably formed simultaneously and thus consist of substantially the same material, e.g., suitable metal or/and semiconductor material, such as polysilicon, doped with the same dopant to substantially the same average net dopant concentration.

Pramanick discloses a field-effect transistor ("FET") having a polycrystalline gate electrode, presumably a gate electrode consisting of doped polycrystalline semiconductor material such as doped polysilicon.

Claim 13, which depends from Claim 1, recites that "the gate electrode comprises multiple gate electrode portions of doped semiconductor material" and that each gate electrode portion is "situated above at least where a different corresponding one of the inversion portions occurs". Claim 13 further recites that each gate electrode portion is "of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion".

Independent Claim 42 is directed to a structure containing a varactor in which a gate electrode overlies a gate dielectric layer above a body region. Similar to Claim 13, Claim 42 recites that the gate electrode comprises "multiple gate electrodes portions of doped semiconductor material" and that each gate electrode portion is "of different conductivity type or/and different average net dopant concentration than each other gate electrode portion".

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Claims 17 - 21 all depend (directly or indirectly) from Claim 13. Claims 44 - 46, 51, and 52 all depend (directly or indirectly) from Claim 42. Accordingly, dependent Claims 17 - 21, 44 - 46, 51, and 52 all require that the gate electrode portions variously differ in conductivity type or/and average net dopant concentration.

Tada does disclose a gate electrode formed with two portions of opposite, and thus different, conductivity types. However, absolutely <u>nothing</u> in Sakai, Tada, Iwamuro, and/or

Pramanick would furnish a person skilled in the art with any suggestion or motivation for configuring capacitance reading electrode 25 in Sakai's MIS varactor as two portions of different conductivity types. Since Sakai lacks an inversion layer consisting of multiple variably appearing portions of different zero-point threshold voltages, Sakai has no need for a gate electrode formed with two portions of different conductivity types.

Modifying capacitance reading electrode 25 in Sakai's MIS varactor so as to consist of two portions of different conductivity types would not improve the varactor performance. The performance of Sakai's MIS varactor would likely be degraded.

Additionally, modifying Sakai's MIS varactor such that capacitance reading electrode 25 consists of two portions of different conductivity types would increase the fabrication complexity and attendant cost. Due to the absence of a performance improvement, increasing the fabrication complexity and cost would not be economically justifiable. A person skilled in the art would absolutely not apply (a) the teachings of Tada to Sakai in an effort to reach the subject matter of any of Claims 13, 17, 18, 42, 44, and 45, (b) the teachings of Tada and Iwamuro to Sakai in an attempt to reach the subject matter of Claim 19 or 46, or (c) the teachings of Tada and Pramanick to Sakai in an effort to reach the subject matter of any of Claims 20, 21, 51, and 52. Claims 13, 17 - 21, 42, 44 - 46, 51, and 52 are thus variously patentable over Sakai, Tada, Iwamuro, and Pramanick.

Claims 19 and 46 respectively depend from Claims 17 and 44 which each recite that "the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region". Claims 19 and 46 each recite that "the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other". Accordingly, each of Claims 19 and 46 require that the metal-containing layer electrically short a pair of gate electrode portions of opposite conductivity types.

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Opposite-conductivity-type portions 4 and 5 of the bottom gate electrode in Tada are not electrically shorted to each other. While Iwamuro discloses that gate electrodes 12 are electrically connected together, Iwamuro does not disclose that electrodes 12 consist of respective doped semiconductor regions of opposite conductivity types. Nor is there any

grounds to believe that gate electrodes 12 in Iwamuro ould reasonably be of <u>opposite</u> conductivity types. Consequently, neither Tada nor Iwamuro discloses the further limitation of Claims 19 and 46 that the metal-containing layer electrically short a pair of gate electrode portions of opposite conductivity types. These differences establish a separate basis for allowing Claims 19 and 46 over Sakai, Tada, and Iwamuro.

Independent Claim 53 is directed to a varactor structure in which a gate electrode overlies a gate dielectric layer above a body region. Claim 53 requires that the gate electrode comprise "multiple gate electrode portions of doped semiconductor material". As amended, Claim 53 further requires that the gate electrode portions be "electrically shorted to one another", that each gate electrode portion be "continuous with at least one other of the gate electrode portions", and that each gate electrode portion be "of different conductivity type or/and different average net dopant concentration than each other gate electrode portion".

As mentioned above, opposite-conductivity-type portions 4 and 5 of Tada's bottom gate electrode are <u>not</u> electrically shorted to each other. Tada fails to meet the limitation of Claim 53 that the gate electrode portions be "electrically shorted to one another". This limitation is, of course, also not met by Sakai. Even if there were some reason or suggestion for combining Sakai and Tada, the combination would <u>not</u> teach the full subject matter of Claim 53. Hence, Claim 53 is patentable over Sakai and Tada.

Claims 57 and 58 both depend (directly or indirectly) from Claim 53 and are thus patentable over Sakai and Tada for the same reasons as Claim 53.

Claims 14 - 16, 43, and 54 - 56 have been rejected under 35 USC 103(a) as obvious based on Sakai and Tada in view of Fratin et al. ("Fratin"), U.S. Patent 5,977,591. This rejection is respectfully traversed.

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Fratin discloses an FET whose source/drain regions are in a lightly doped drain configuration. Gate electrode 8 of Fratin's FET has mid-portion 13 which solely overlies channel region 7 and is of the same conductivity type as well (body region) 3. Gate electrode 8 has a pair of extensions 14 which are continuous with mid-portion 13 and which respectively extend over source/drain regions 4 and 5. Gate-electrode extensions 14 are either of opposite conductivity type to mid-portion 13 (and well 3) or of the same conductivity type as, but more lightly doped than, mid-portion 13.

Claims 14, 43, and 54 which respectively depend from Claims 13, 42, and 53, each recite that "the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations". Although extensions 14 of gate electrode 8 in Fratin are, in one embodiment, doped more lightly than mid-portion 13, absolutely nothing in Sakai, Tada, and/or Fratin would provide a person skilled in the art with any reason or motivation for configuring capacitance reading electrode 25 in Sakai's MIS varactor as multiple portions of the same conductivity type but different average net dopant concentrations. Inasmuch as Sakai lacks an inversion layer consisting of multiple variably appearing portions of different zero-point threshold voltages, Sakai has no need for a gate electrode formed with multiple portions of the same conductivity type but different average net dopant concentrations.

Modifying Sakai's capacitance reading electrode 25 so as to consist of multiple portions of the same conductivity type but different average net dopant concentrations would not improve the performance of Sakai's MIS varactor. The varactor performance would likely be degraded.

Modifying Sakai's MIS varactor so that capacitance reading electrode 25 consists of multiple portions of a same conductivity type but different average net dopant concentrations would also increase the manufacturing complexity and cost. Without a performance improvement, increasing the manufacturing complexity and cost would not be economically justifiable. A person skilled in the art would absolutely not apply the teachings of Tada and Fratin to Sakai in an effort reach the subject matter of any of Claims 14, 53, and 54. Accordingly, Claims 14, 43, and 54 are patentable over Sakai, Tada, and Fratin.

Claims 15 and 16 both depend from Claim 14. Claims 55 and 56 both depend from Claim 54. Hence, Claims 15, 16, 55, and 56 are patentable over Sakai, Tada, and Fratin for the same reasons as Claims 14 and 53.

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Claims 22 - 24, 47 - 49, 59, and 60 have been rejected under 35 USC 103(a) as obvious based on Sakai and Tada in view of Hattori. Claims 25 and 50 have been rejected under 35 USC 103(a) as obvious based on Sakai, Tada, and Hattori in view of Iwamuro. Claims 26 and 27 have been rejected under 35 USC 103(a) as obvious based on Sakai, Tada, and Hattori in view of Pramanick. These rejections are respectfully traversed.

Claims 22, 47, and 59, which respectively depend from Claims 1, 42, and 53, are directed to embodiments, such as that of application Fig. 15, in which gate electrode portions of opposite conductivity types are combined with gate dielectric portions of different thicknesses. In particular, Claims 22, 47, and 59 each specify that "the gate dielectric layer comprises a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion", that "the gate electrode portions comprise (a) a first gate electrode portion" of doped semiconductor material "of opposite conductivity type to the body region and (b) a second gate electrode portion" of doped semiconductor material "of the same conductivity type as the body region", and that the first gate electrode portion overlies "the first and second gate dielectric portions".

Claims 23 - 27 all depend from Claim 22. Claims 48 - 50 all depend from Claim 47. Claim 60 depends from Claim 59. As a result, dependent Claims 23 - 27, 48 - 50, and 60 all require that gate electrode portions of opposite conductivity types be combined with gate dielectric portions of different thicknesses.

While (a) Tada discloses a gate electrode formed with portions of opposite conductivity types and (b) Hattori discloses a gate dielectric layer formed with portions of different thicknesses, absolutely <u>nothing</u> in Sakai, Tada, Hattori, or/and Pramanick would furnish a person skilled in the art with any suggestion or motivation (i) for configuring Sakai's capacitance reading (gate) electrode 25 as two portions of opposite conductivity types and (ii) for configuring Sakai's insulating (gate dielectric) layer 24 as two portions of different thicknesses. Since Sakai lacks an inversion layer consisting of multiple variably appearing portions of different zero-point threshold voltages, Sakai has <u>no need</u> for (i) a gate electrode formed with two portions of opposite conductivity types and/or (ii) a gate dielectric layer consisting of multiple portions of different thicknesses.

Modifying (i) Sakai's capacitance reading electrode 25 to consist of two portions of opposite conductivity types and (ii) Sakai's insulating layer 24 to consist of two portions of different thicknesses would increase the fabrication complexity and cost <u>without</u> producing any performance improvement. The performance of a so-modified version of Sakai's MIS varactor would likely be <u>degraded</u>. Consequently, increasing the fabrication cost and complexity would not be economically justifiable. A person skilled in the art would absolutely <u>not</u> apply (a) the teachings of Tada and Hattori to Sakai in an effort to reach the

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subject matter of any of Claims 22 - 24, 47 - 49, 59, and 60, (b) the teachings of Hattori and Iwamuro to Sakai in an attempt to reach the subject matter of Claim 25 or 50, or (c) the teachings of Tada, Hattori, and Pramanick to Sakai in an effort to reach the subject matter of Claim 26 or 27. Claims 22 - 27, 47 - 50, 59, and 60 are thus variously patentable over Sakai, Tada, Hattori, Iwamuro, and Pramanick.

Claims 25 and 50 each require that the gate electrode include a metal-containing layer for electrically shorting two gate electrode portions of opposite conductivity types. Due to their dependence from amended Claim 53, Claims 59 and 60 similarly require that two gate electrode portions of opposite conductivity types be electrically shorted together. As indicated above, neither Tada nor Iwamuro discloses or suggests the electrical shorting of two gate electrode portions of opposite conductivity types. Even if there were some reasonable basis for combining Tada and possibly Iwamuro with Sakai and Hattori, the combination would <u>not</u> teach the full subject matter of any of Claims 25, 50, 59, and 60. This is a further reason why Claims 25 and 50 are patentable over Sakai, Tada, Hattori, and Iwamuro, and also a further reason why Claims 59 and 60 are patentable over Sakai, Tada, and Hattori.

Claims 28, 31, 38, and 41 have been rejected under 35 USC 103(a) as obvious based on Sakai and Hattori in view of Maszara et al. ("Maszara"), U.S. Patent Publication 2003/0178689 A1. Claim 30 has been rejected under 35 USC 103(a) as obvious based on Sakai in view of Watanabe, U.S. Patent 4,003,009.

Maszara discloses an FET whose gate electrode is divided into two portions having different work functions.

Watanabe discloses a pair of electronic circuits in which an inductor, a resistor, and a varactor are arranged in series.

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Claims 28, 30, and 31 all depend from Claim 1 and thus require an inversion layer comprising multiple portions of different zero-point threshold voltages of like sign. As pointed out above, Sakai does <u>not</u> meet this inversion-portion requirement. Accordingly, a person skilled in the art would have absolutely <u>no</u> reason for applying the teachings of Hattori, Maszara, or/and Watanabe to Sakai. Claims 28, 30, and 31 are thus variously patentable over Sakai, Hattori, Maszara, and Watanabe.

Claims 38 and 41 respectively depend from independent Claims 34 and 39. Even if there were some motivation or suggestion for combining Maszara with Sakai and Hattori utilized in rejecting Claim 34, the combination of Sakai, Hattori, and Maszara would not make Claim 34 unpatentable. Since Claim 38 depends from Claim 34, Claim 38 is likewise patentable over Sakai, Hattori, and Maszara. Similarly, combining Maszara and Hattori with Sakai employed in rejecting Claim 39 would not make Claim 39 unpatentable even if there were some reason or incentive for combining Sakai, Hattori, and Maszara. Due to its dependence from Claim 39, Claim 41 is patentable over Sakai, Hattori, and Maszara.

Claims 6 - 9, 13 - 28, 30, 31, 34 - 38, and 41 - 52, all of which have been rejected under 35 USC 103(a) as obvious based on Sakai and one or more other references, are <u>also</u> patentable over the applied art for the following <u>separate</u> reasons. As mentioned above, independent Claims 1 and 39 each specify that the claimed structure includes "further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor" and that "the plate and body electrodes" are "situated in the capacitance signal path". The same limitation is recited in each of independent Claims 34 and 42. Claims 1, 34, 39, and 42 thus each require that the <u>plate</u> electrode be situated in the capacitance signal path of the electronic circuitry that employs the varactor recited in those claims.

As also mentioned above, Sakai measures the capacitance of its MIS varactor between capacitance reading electrode 25 and bottom electrode 18. Since the Examiner has analogized electrodes 25 and 18 respectively to the gate and body electrodes of the present claims, "gate" electrode 25 and "body" electrode 18 of Sakai's MIS varactor would be situated in the capacitance signal path of electronic circuitry which utilizes Sakai's MIS varactor.

Sakai's control electrode 16 (or 17) which the Examiner has analogized to the plate electrode of the present claims would <u>not</u> be situated in the electronic circuitry's capacitance signal path. The requirement of each of Claims 1, 34, 39, and 42 that the plate electrode be situated in the capacitance signal path of the further electronic circuitry which utilizes the recited varactor is thus <u>not explicitly</u> or <u>inherently</u> met in Sakai. For this reason, Claims 34 - 38 and 42 - 52 along with Claims 6 - 9, 13 - 28, 30, 31, and 41 which variously depend from Claims 1 and 39 are separately patentable over the applied art.

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New Claims 69 and 70 both depend (directly or indirectly) from Claim 53. Claim 69 requires that "the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other". Inasmuch as Sakai, Tada, and Iwamuro have been applied against dependent claims, such as Claim 19, which present this requirement, Claim 69 and its dependent Claim 70 are patentable over Sakai, Tada, and Iwamuro for the same reasons that Claim 53 is patentable over Sakai and Tada.

New Claims 71 and 72 likewise both depend (directly or indirectly) from Claim 53. Claim 71 requires that "the doped semiconductor material of the gate electrode portions comprise doped non-monocrystalline semiconductor material". Since Sakai, Tada, and Pramanick have been applied against dependent claims, such as Claim 20, which recite this semiconductor material requirement, Claim 71 and its dependent Claim 72 are patentable over Sakai, Tada, and Pramanick for the same reasons that Claim 53 is patentable over Sakai and Tada.

New Claims 73 and 74 depend (directly or indirectly) from Claim 59 and are patentable over Sakai, Tada, and Hattori for the same reasons as Claim 59.

In short, all of pending Claims 1 - 60 and 69 - 74 have been shown to be patentable over the applied art. Accordingly, Claims 1 - 60 and 69 - 74 should be allowed so that the application may proceed to issue.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

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